High Performance Computing Systems and Enabling Platforms (SPA), a.a. 2009-10

Some integrations to course material and literature for optional contributions

The Course Page contains some papers to be used in different ways, as explained below.

Flynn's classification of parallel architectures

A short paper that resumes the characteristics of the well-known Flynn's classification (SISD, SIMD, MISD, MIMD), which represents a piece of history and culture in computer architecture. To be used as a *general reference*.

Drepper's monograph on memory hierarchies

This long and detailed report discusses, in a very clean and sound way, the impact of memory and caching technologies on program design and performance.

The following sections can be used *in support to prerequisites* on computer architecture, memory technology, hierarchies and caching:

- introduction of Section 2 (Commodity hardware today),
- Section 3 (CPU caches): introduction, 3.1, 3.2, 3.3.1, 3.3.2, 3.3.3, 3.3.5, 3.4, 3.5,
- Section 4 (Virtual memory): 4.1, 4.2, 4.3,
- students interested in the physical structure of memories can consult Sections 2.1, 2.2, 2.3. This part could be useful to confirm some typical values of memory access time, latency and bandwidth, as known from the Pisa undergraduate course on Computer Architecture, and as used in SPA.

The following sections are used as *official material for the SPA exam*:

- Section 3.3.4 (Multiprocessor support),
- Section 4.4 (Virtualization),
- Section 5 (NUMA support),
- Section 8 (Upcoming technology).

The following sections can be used for *as optional contributions to the SPA exam (reports to be submitted)*, possibly splitted into more than one contribution:

- Section 6 (What programmers can do),
- Section 7 (Memory performance tools).

Survey on Explicit Multithreading

The initial part of the paper by Ungerer, Robic and Silc (2003) is used as *official material for the SPA exam*:

- Section 1,
- Section 2.

The remaining sections can be used for *as optional contributions to the SPA exam (reports to be submitted)*, possibly integrated with references to more recent processors:

- Section 3, 4, 5 (Interleaved and blocked multithreading),
- Section 6, 7 (Simultaneous multithreading).

Cache Coherence Protocols

The initial part of the paper by Pong and Dubois (1997) is used as *official material for the SPA exam*:

- Section 1,
- Section 2,

along with the above-mentioned parts of Drepper's paper.

The remaining sections can be used for *as optional contributions to the SPA exam (reports to be submitted)*, possibly splitted into more than one contribution.

Compiler transformations for high-performance computing

Though the importance and nature of compiler optimizations are discussed and exemplified in several parts of the course, a complete, systematic and detailed description of all the compiler optimizations is out of scope of the SPA course (it could be the subject of a subsidiary course or of the Master Thesis).

The classical survey paper by Bacon, Graham and Sharp (1994) contains the majority of the state of the art techniques (despite the publication year, very few novelties have been introduced in the meantime).

It can be used for *as optional contributions to the SPA exam (reports to be submitted)*, splitted into more than one contribution.

Existing multicore products and trends

Multicore technology will be studied in the context of parallel architectures. During these parts of the SPA course, several concepts and techniques will be exemplified by mentioning existing multicore products.

For a more deepen descrition and treatment, the following documents can be used for *as optional contributions to the SPA exam (reports to be submitted)*, possibly integrated with references to more recent processors and/or research results:

- **Multicore computing – the state of the art** (Faxen ed, 2008),
- **Summary of multicore hardware and programming model investigations** (Pedretti et al, 2008).