

Fabrizio Luccio

## Chip functioning and manufacturing

Main sources for data and images:

IEEE Computer

IEEE Spectrum

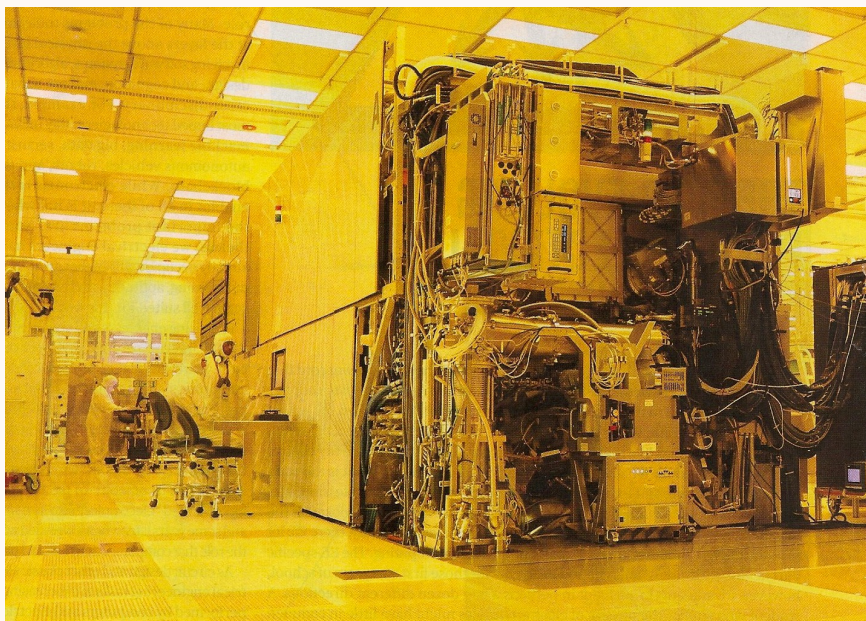
Communications of the ACM

Foundries on-line documents

U. Berkeley: Lecture Notes for EL ENG X481

C. Mead, L. Conway: Introduction to VLSI Systems

Wikipedia (images)

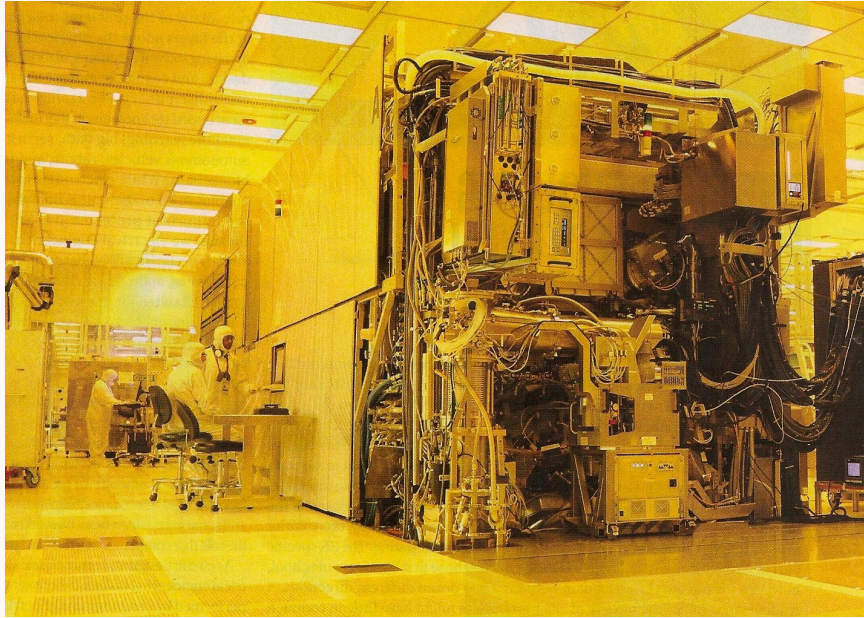


ASML NXE:3300B

2018  
a year of innovation



Broadcom BCM47755



ASML NXE:3300B

2018  
a year of innovation



Broadcom BCM47755





## March 1949 A prediction

Engineers and mathematicians are like airplane designers. Models in use are already long outmoded by those on the drawing boards. Where a calculator like the ENIAC today is equipped with 18,000 vacuum tubes and weighs 30 tons, computers in the future may have only 1000 vacuum tubes and perhaps weigh only 1½ tons.

Though never completely satisfied with performance, scientists get a happy gleam in their eyes when they contemplate the high-speed electronic calculating machines of today and the future.

One of them puts it this way: "Just one of these machines will do in a few hours what a human mathematician couldn't do with a million pencils in a hundred lifetimes."

**Transistors** appeared in 1947 at Bell Labs, with first use in electronic circuits in the 50's.

**Integrated circuits** (whole circuits on a single semiconductor) were proposed in 1957 at Texas Instruments, with first implementation in 1958.

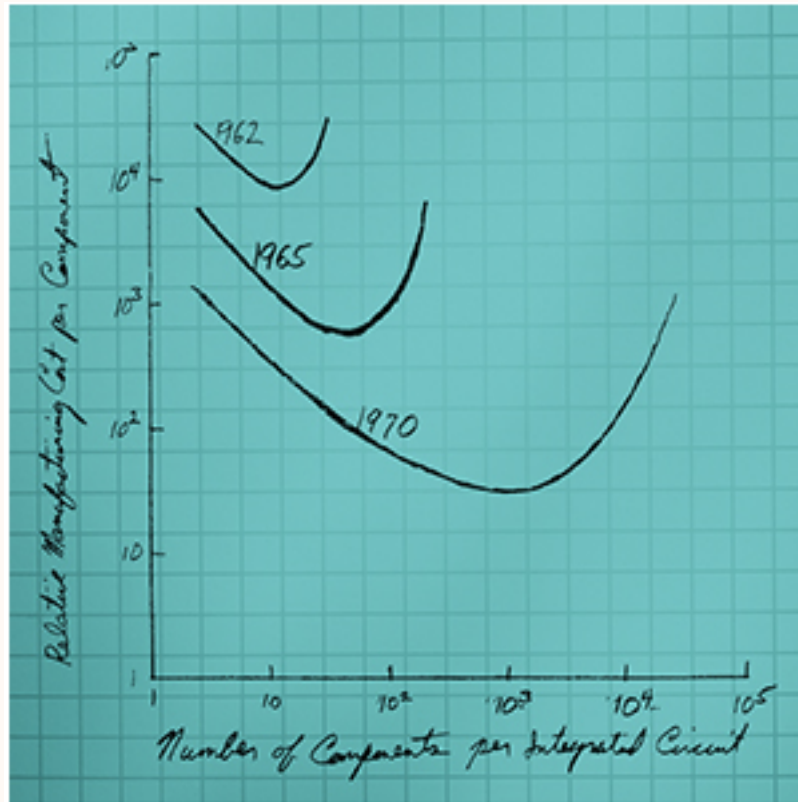
1965

Gordon Moore  
Fairchild



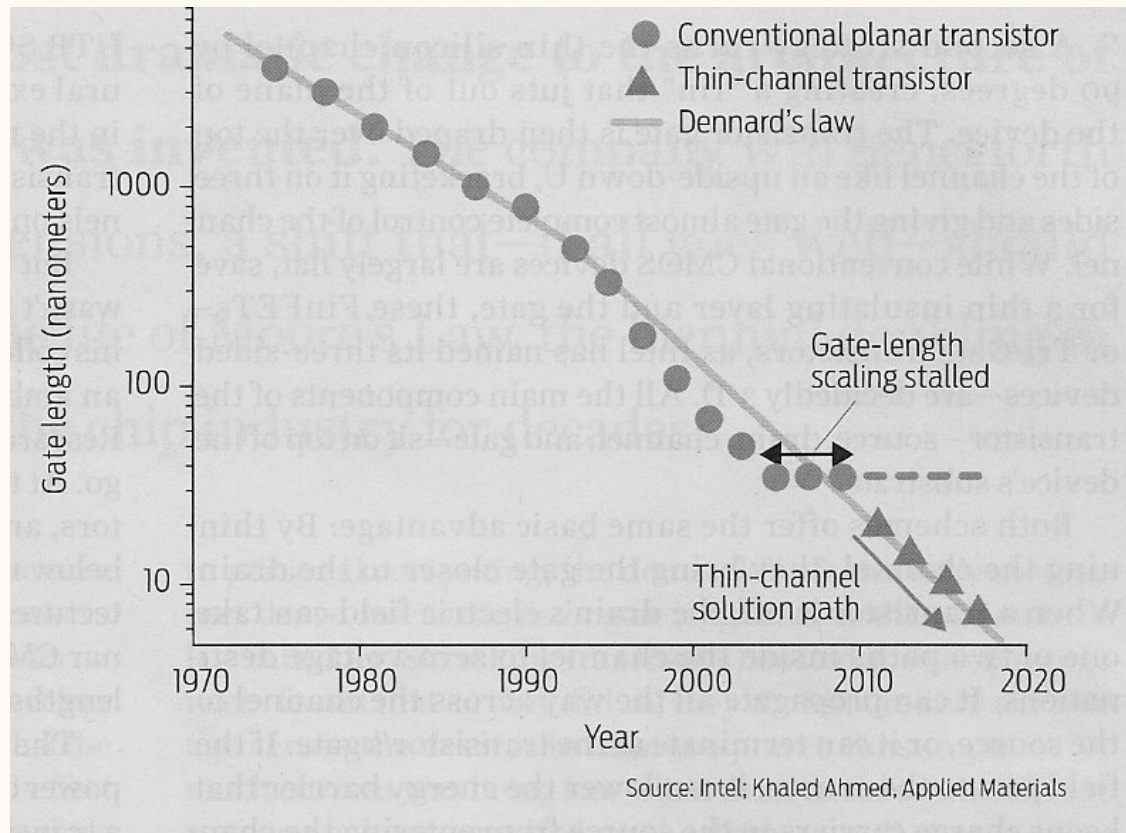
the circuits of computers, mobile phones, and other control systems will be regulated by a yearly doubling in the number of components that can be economically packed in an integrated circuit

G.E. Moore. Cramming More Components onto Integrated Circuits. *Electronics Magazine*. **38** (8), 114-117 (1965).



Economics was at the core of Moore's 1965 paper. For any particular generation of manufacturing technology, there is a cost curve. The cost of making a component declines the more you pack onto an integrated circuit, but past a certain point, yields decline and costs rise. The **sweet spot**, where the cost per component is at a minimum, moves to more and more complex integrated circuits over time.

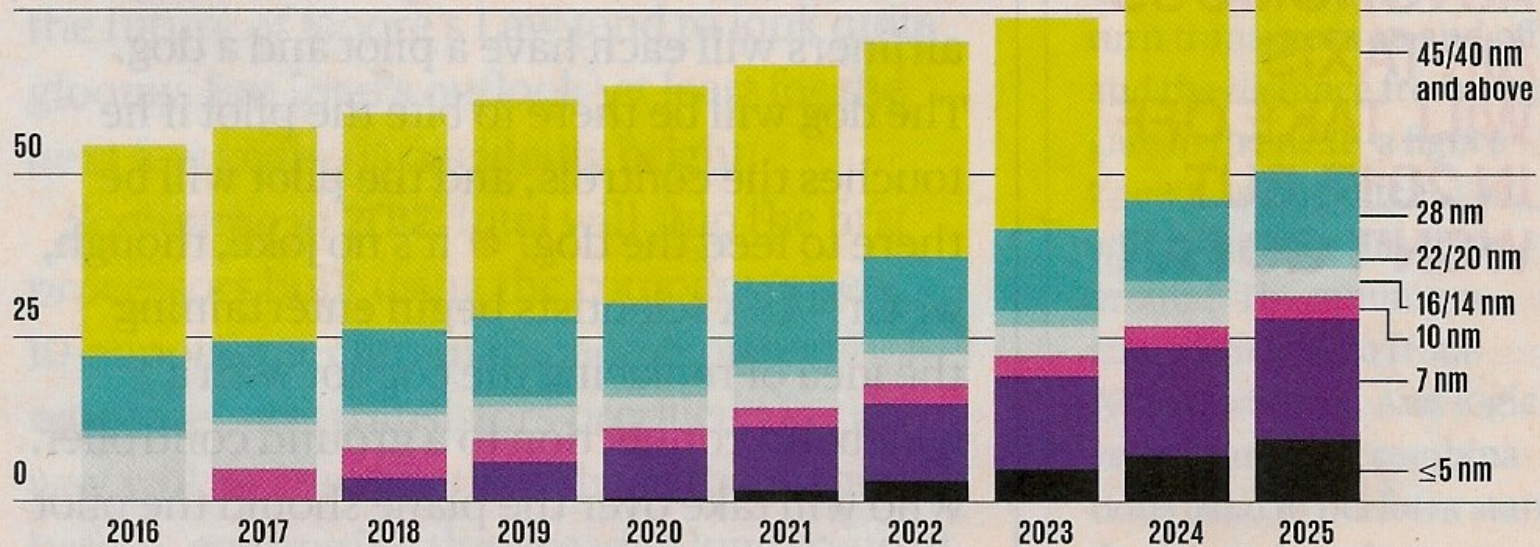
# INTEL



Transistor density at the end of 2017:  $10^{10}/\text{cm}^2$



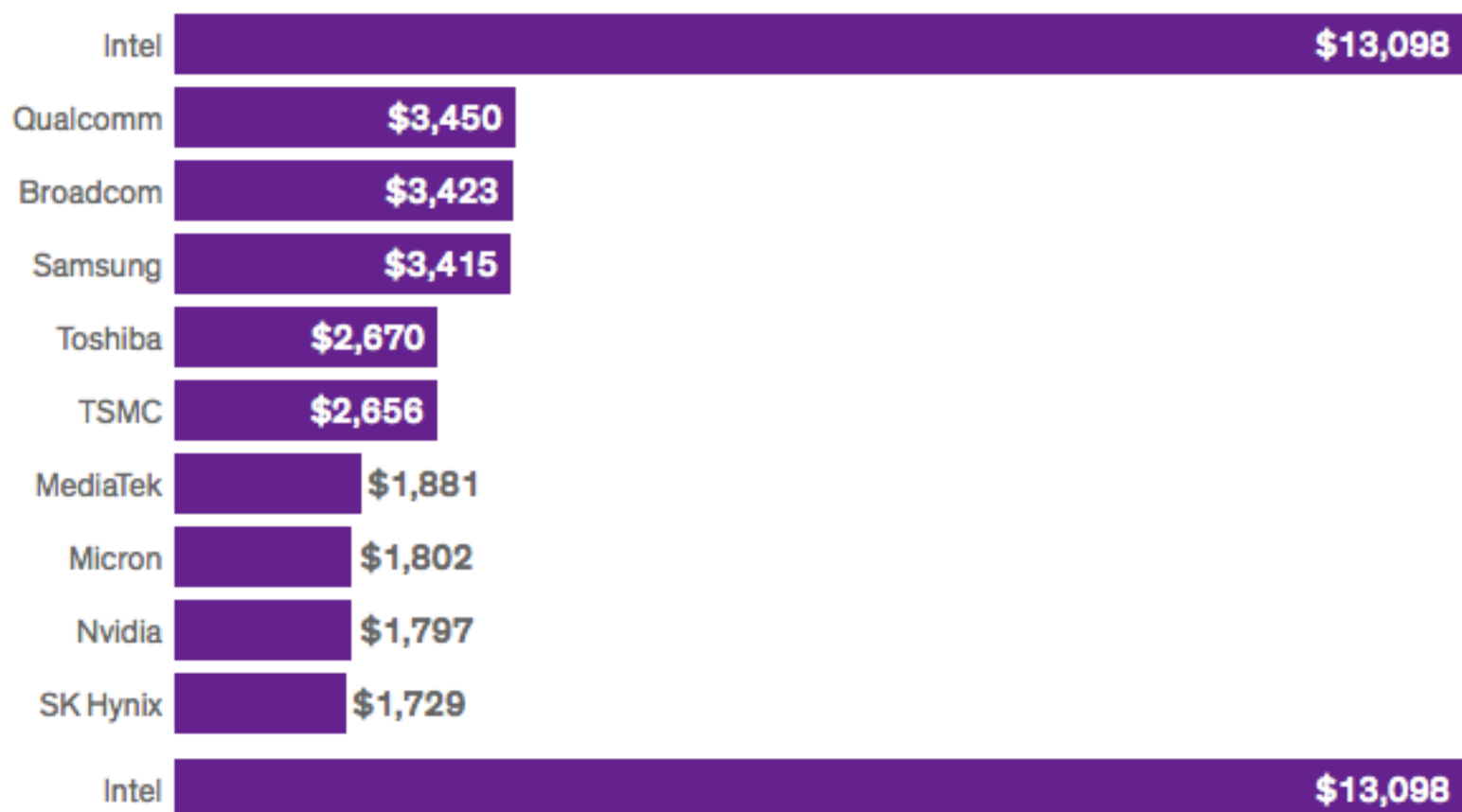
US \$, BILLIONS  
75



**THE EVOLVING FOUNDRY MARKET:** Chips built with 10-nanometer technology will come first. But International Business Strategies projects that Apple and others will be drawn to the next node in line: 7 nm.

## Top Semiconductor R&D Spenders by US Dollars

2017 R&D spending, in millions of US dollars



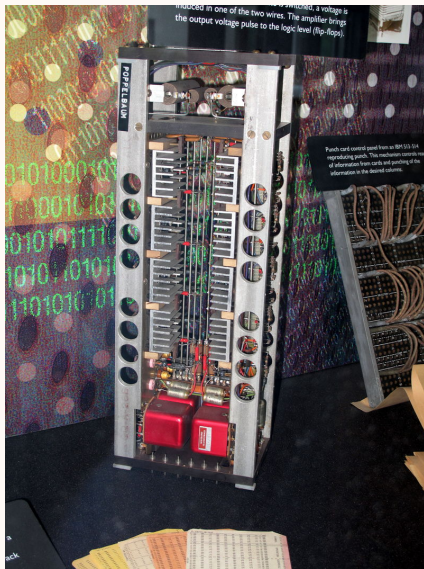
1966 **ILLIAC III**: the first big parallel computer

Bruce McCormik  
University of Illinois



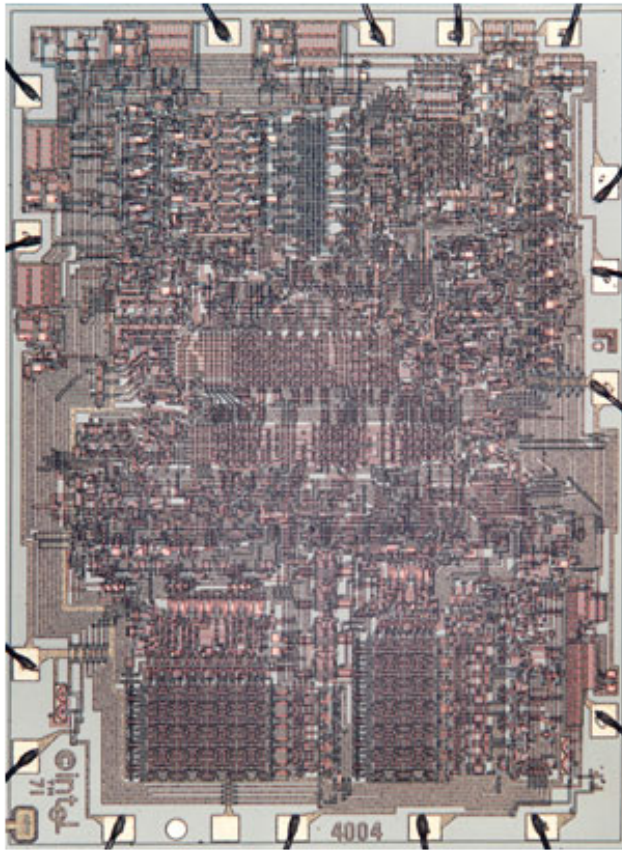
Leader of the project of ILLIAC III, a fine-grained SIMD machine (data level parallelism but not concurrency) built inside the University of Illinois.

ILLIAC III was built for image processing of bubble chamber experiments on nuclear particles, and it was also used on biological images.



The PAU (Pattern Articulation Unit) was the core parallel-processing element of the machine.





## INTEL 4004 (1970)

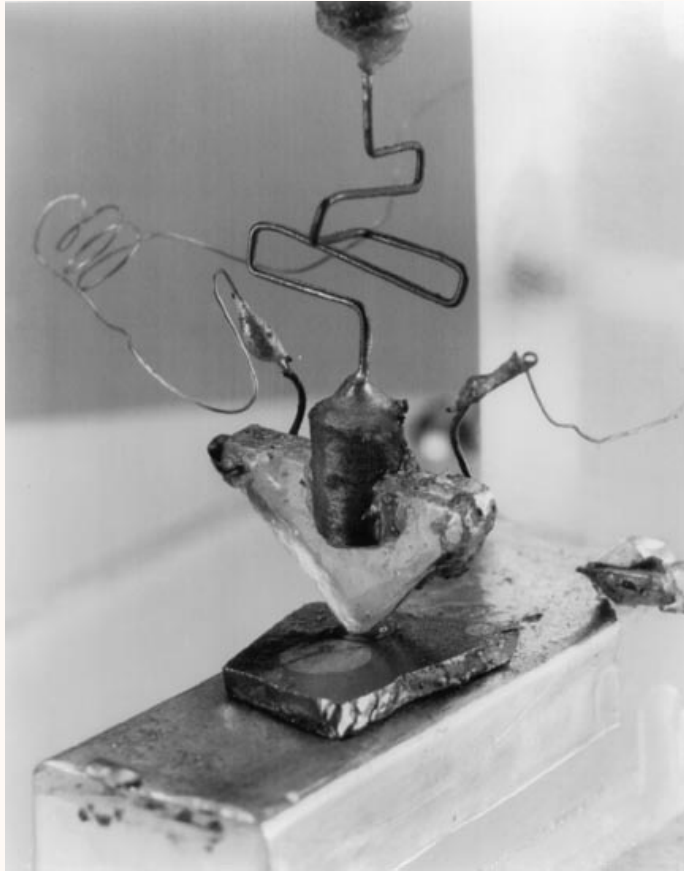
2300 transistors  
10 $\mu$ m minimal feature



Federico Faggin, Ted Hoff Jr., Stanley Mazor



# Transistor: the basic component

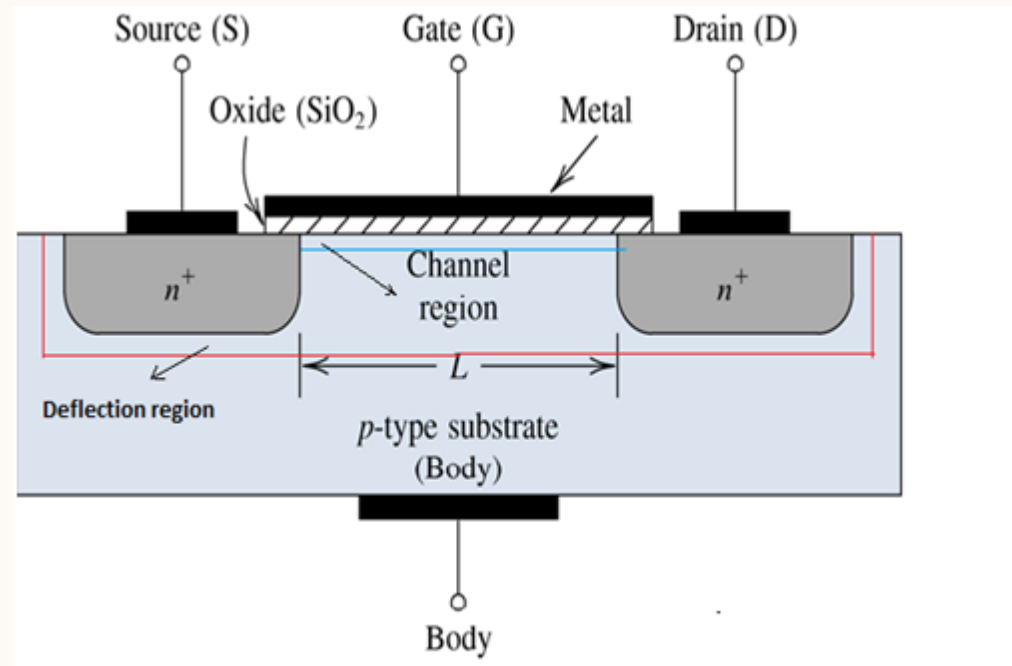


The first transistor  
Bell Labs, 1947



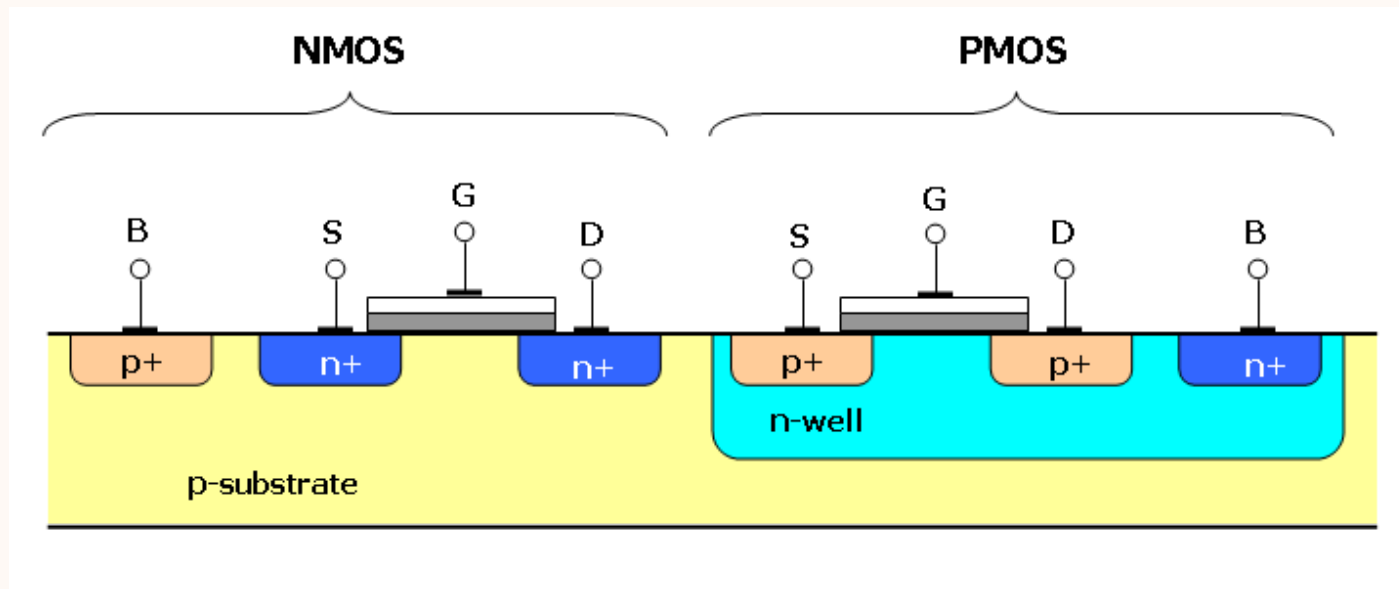
Brattain, Bardeen, Shockley

In 1959 Kahng and Atalla at Bell Labs invented the MOSFET transistor as an offshoot to the FET design patented by Lilienfeld in 1925  
**MOSFET** stands for **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor



NMOS transistor

In 1967 Wanlas proposed the CMOS technology: twice as many transistors, but much less energy required. CMOS stands for Complementary MOS



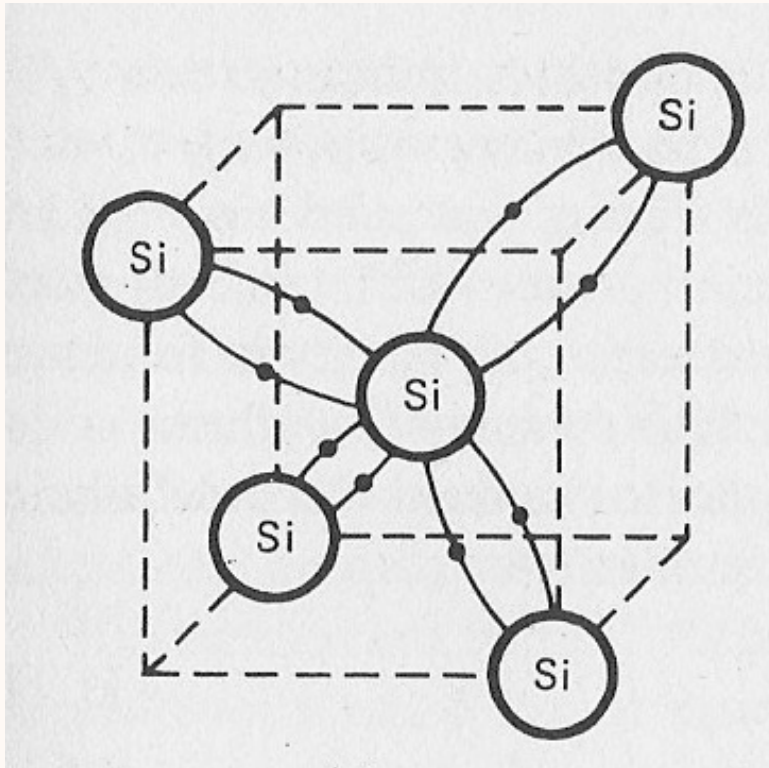
## Silicon ingots (diameter 30 cm)



Mono-crystalline  
Wafer thickness 0.75 mm



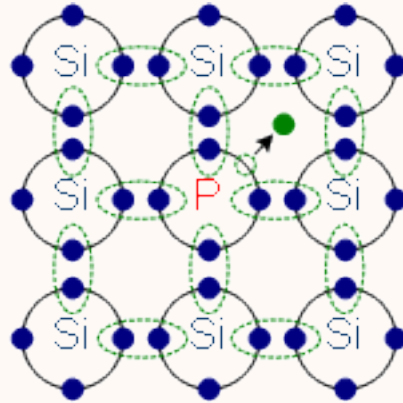
Poly-crystalline  
Wafer thickness 0.2 mm



$10^{22}$  atoms/cm<sup>3</sup>

Van der Waals radius  
210 pm = 0.21 nm

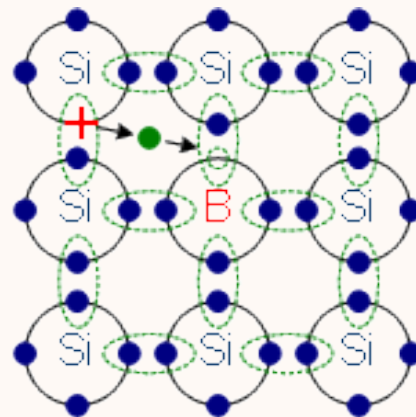




The phosphorus atom donates its fifth valence electron. It acts as a free charge carrier.

n-silicon doped with phosphorus

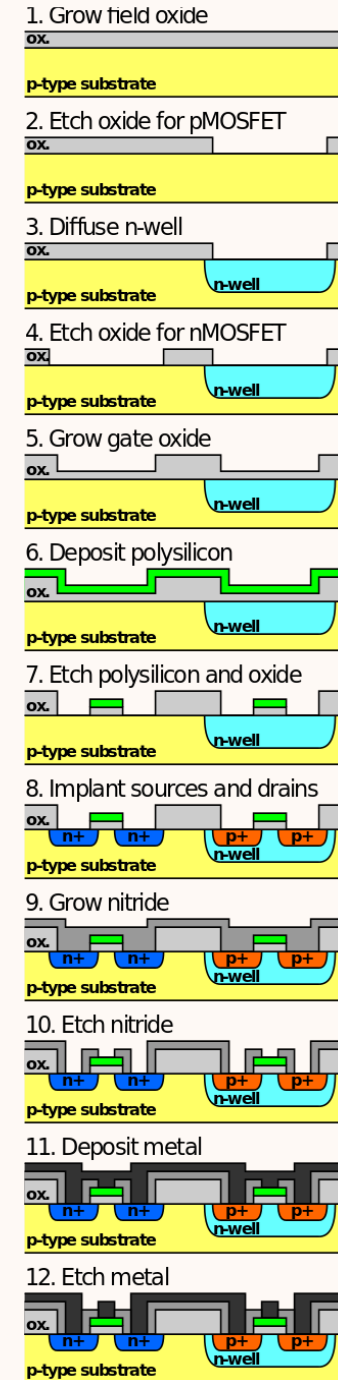
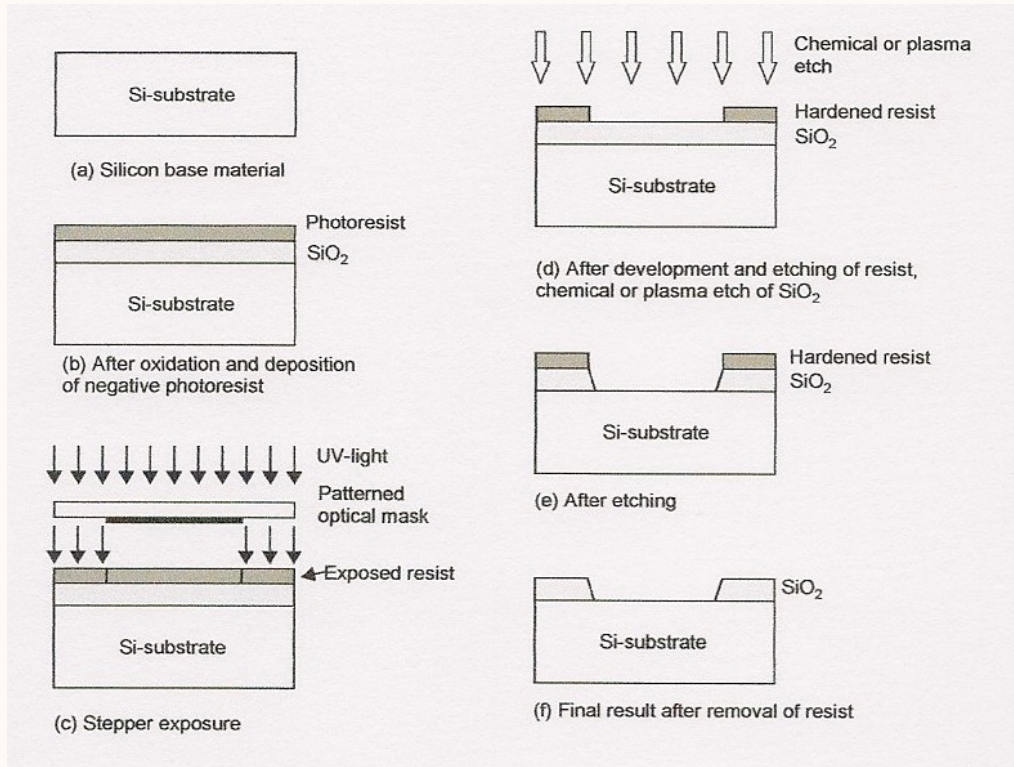
impurity 1 atom every  $10^9$   
doping  $10^{15}$  atoms/cm<sup>3</sup>



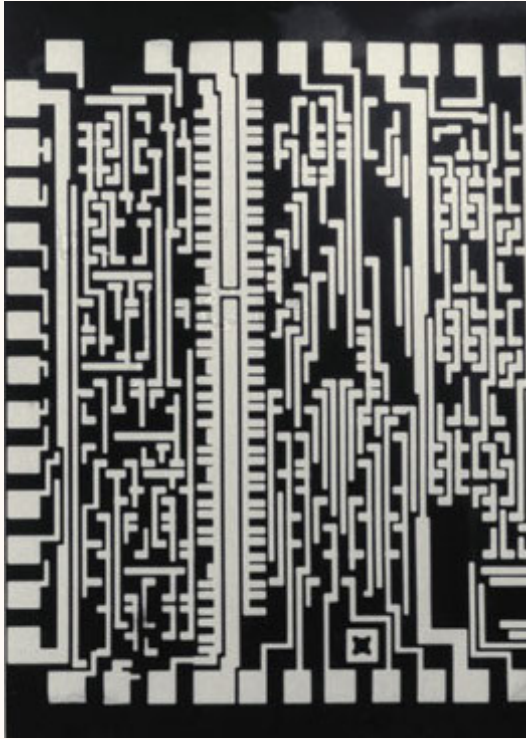
The free place on the boron atom is filled with an electron. Therefore a new hole („defect electron“) is generated. This holes move in the opposite direction to the electrons

p-silicon doped with boron

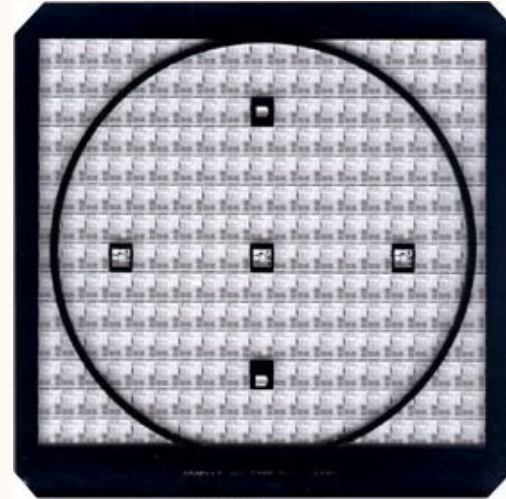
# Lithography



# Masks



individual chip



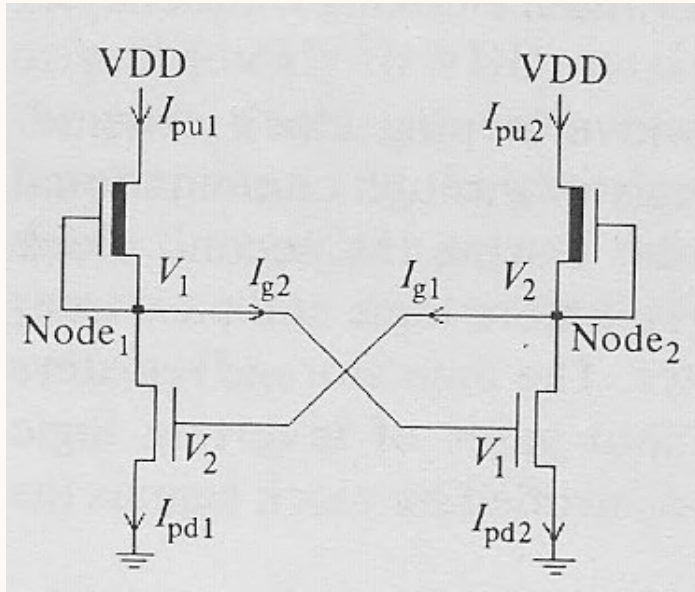
wafer

Several tens of layers may be piled up.

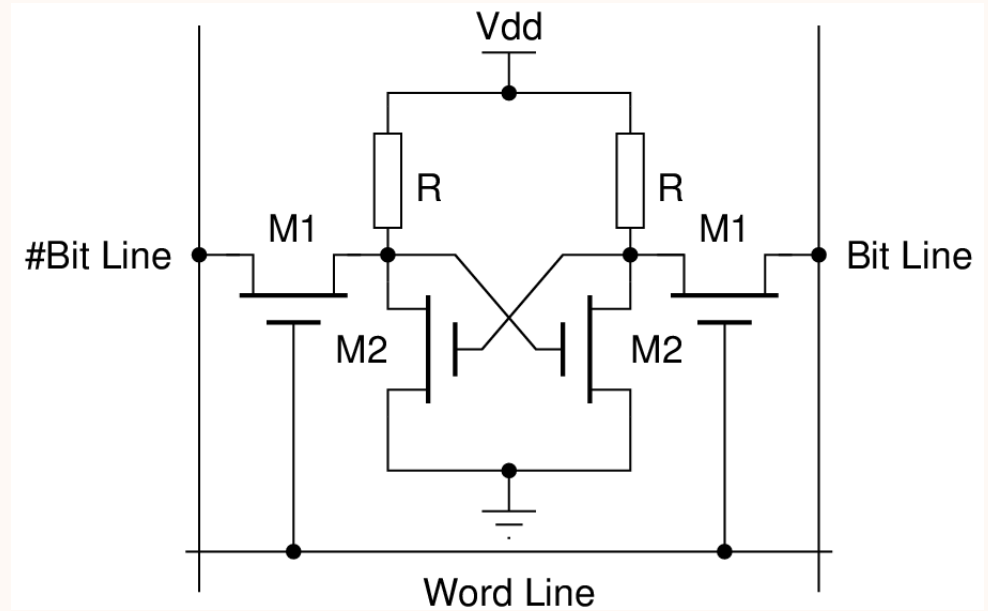
The highest ones containing metallic connections may be thirty or more: in fact over ten kilometers of wiring are contained today in a chip area of  $1 \text{ cm}^2$ .





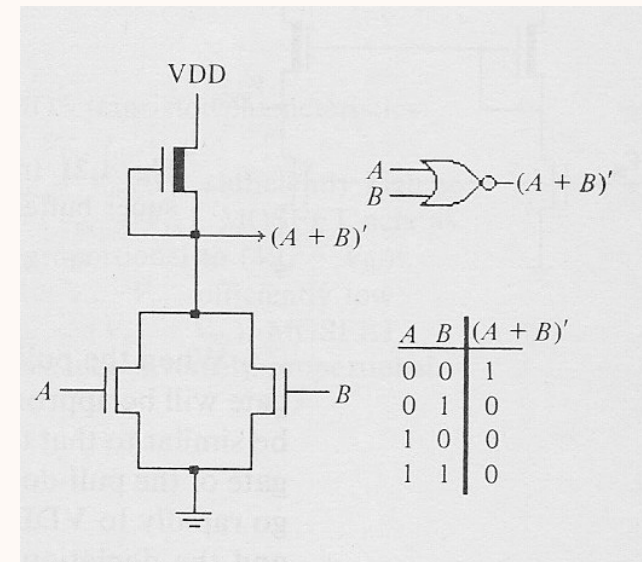
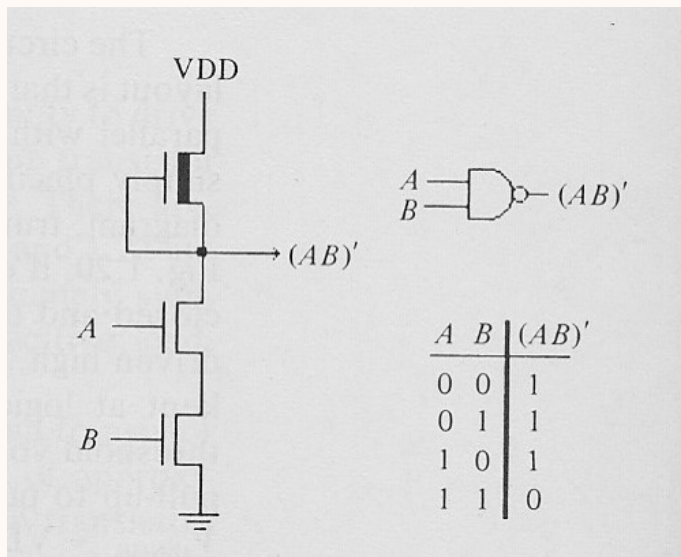


Coupled inverters

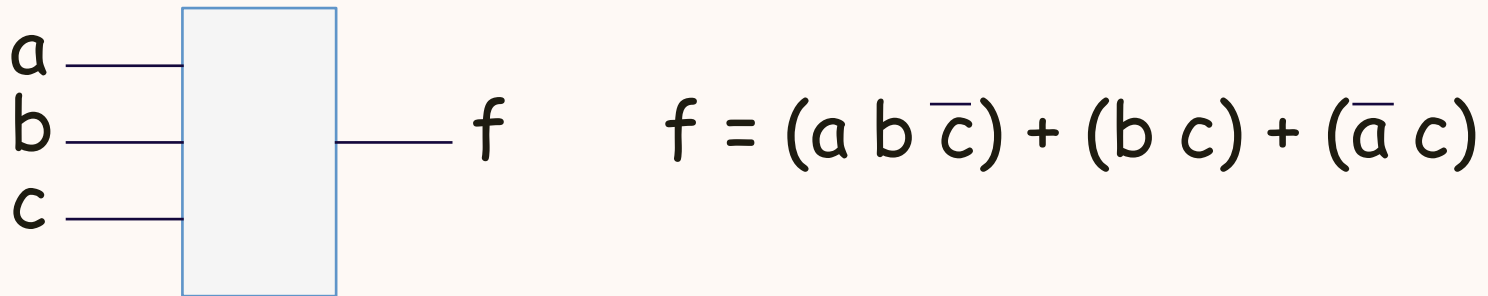


RAM cell

# NAND e NOR



Any combinatorial function  $f$  can be represented in SOP form

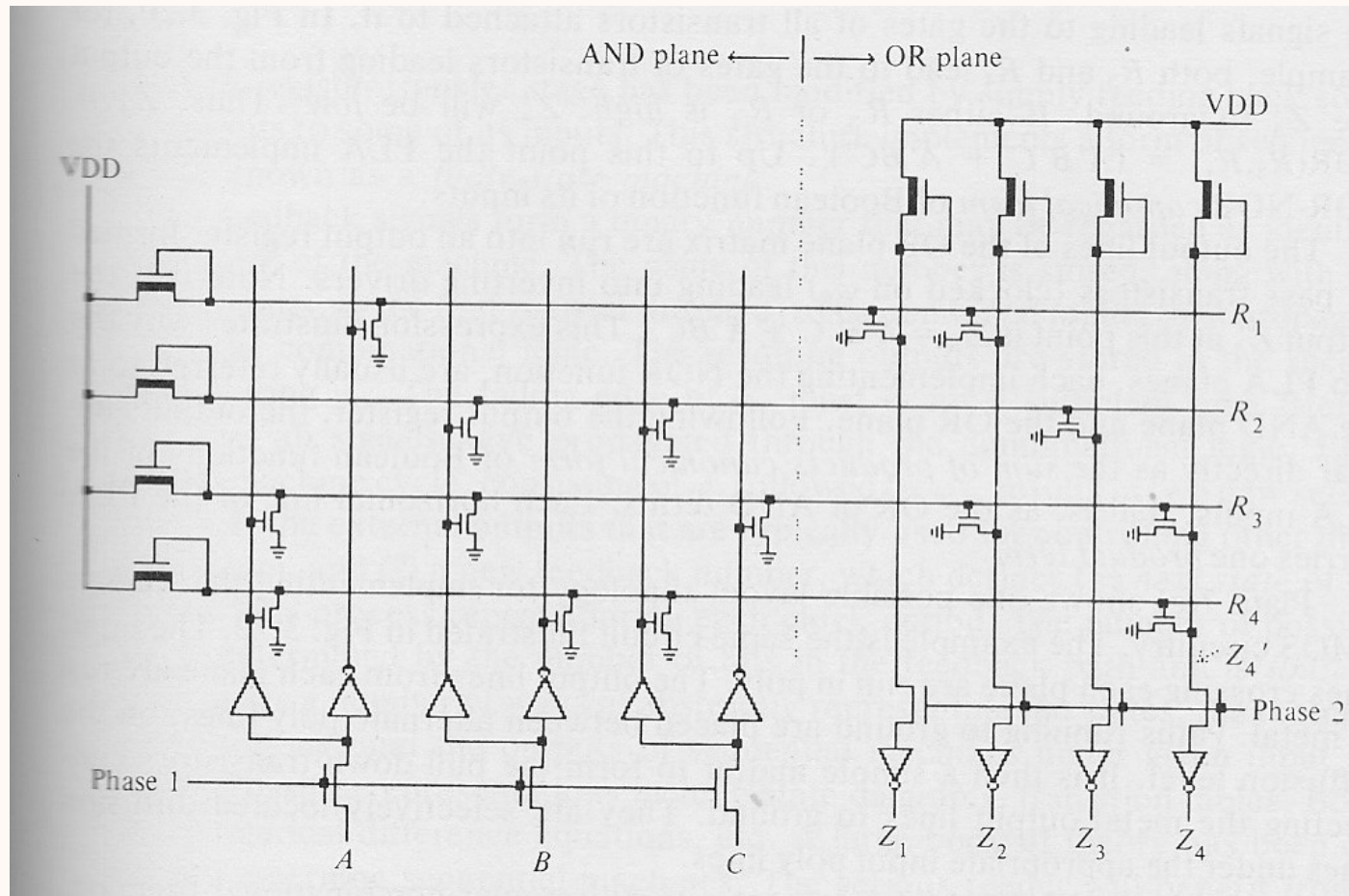


$$f = (a b \bar{c}) + (b c) + (\bar{a} c)$$

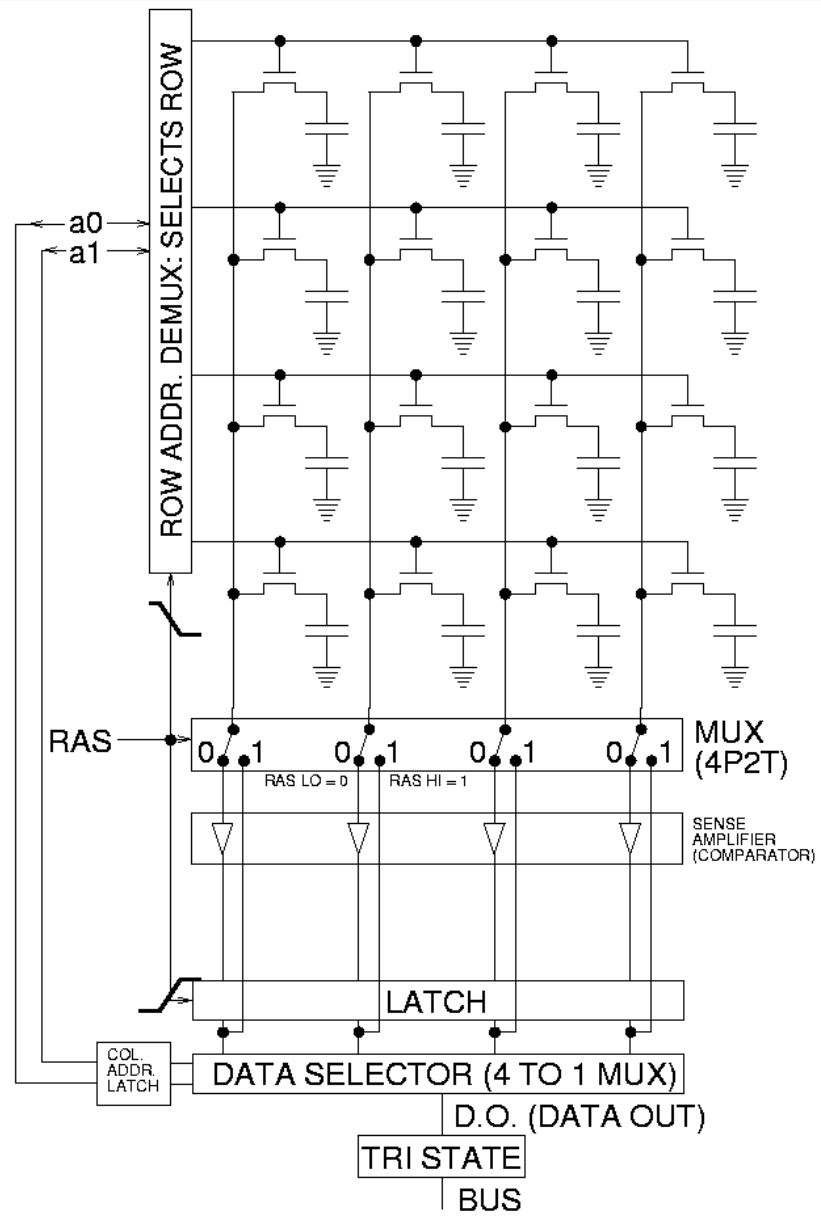
$$(a b \bar{c}) + (b c) + (\bar{a} c)$$
$$= (a|b|\bar{c}) | (b|c) | (\bar{a}|c)$$

SOP forms are immediately transformed into two-level NAND forms. POS forms are transformed in two-level NOR forms.

# PLA

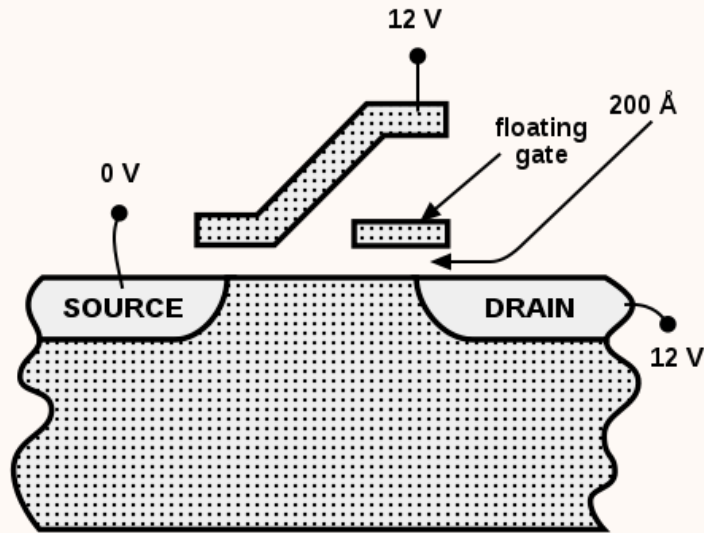


# DRAM





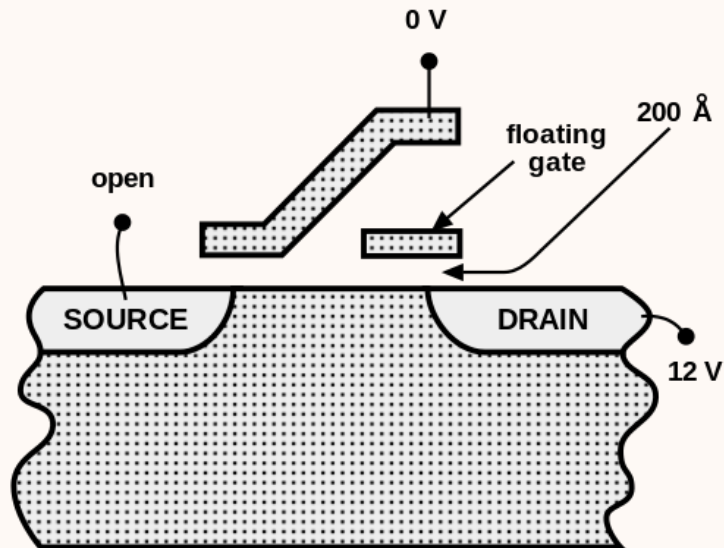
Programming via hot electron injection



## Flash memory

Below the control gate, an insulated floating gate is separated from the channel by an extra-thin insulator layer

Erase via tunneling



Works on quantum tunneling effect

# Parameters controlling functioning

The main electric function in transistor commutation is loading and unloading the capacitance  $C$  arising between gate and substrate, through the connection resistance  $R$ . Power dissipation occurs through resistances, mainly in the source-drain path. Moreover many parasitic capacitances and resistances exist

$$v_g(t) = V_g(1 - e^{-t/RC}) \quad \text{where } RC \text{ is the circuit } \textit{time constant}$$

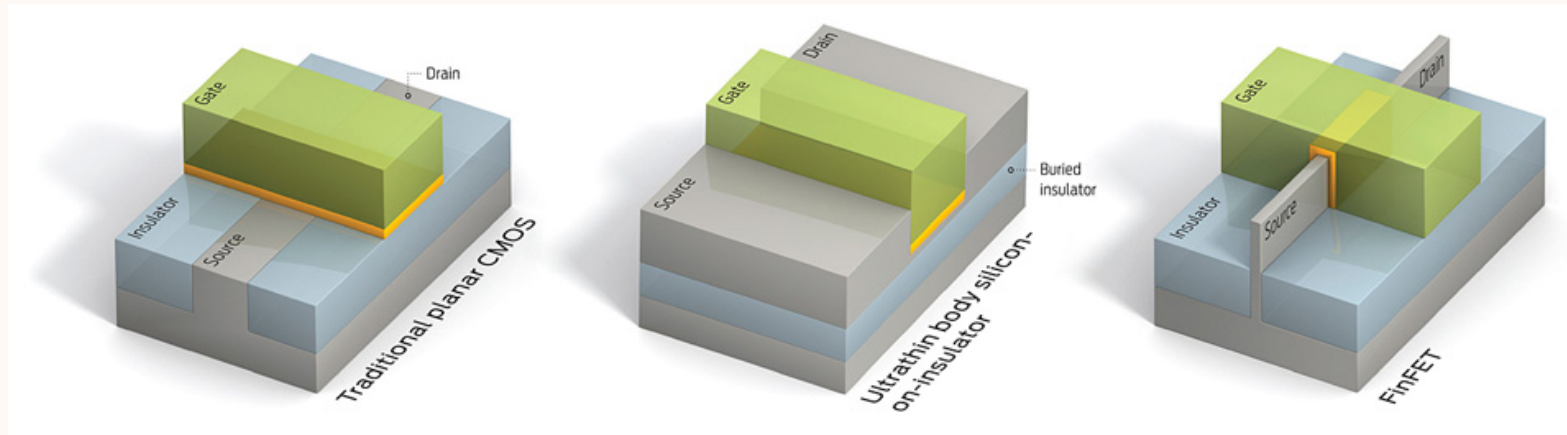
$$w = \sum Ri^2 \quad e = wt$$

The smaller the circuit parameters, the higher the speed and the smaller the energy consumption

$$i = C \, dv/dt$$

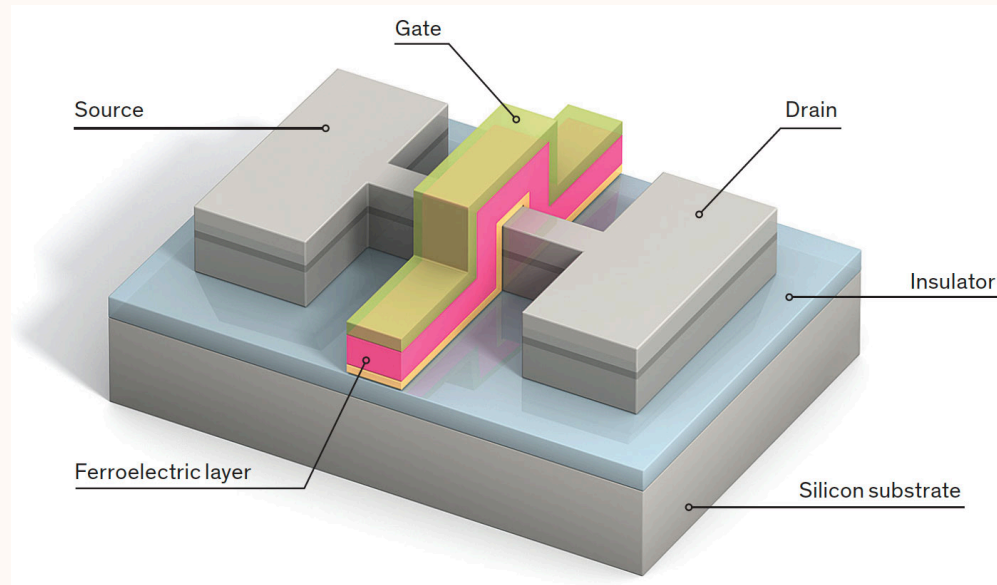
The the deeper the voltage front,, the higher the current and the source power

# From PLANAR to FINFET



## Ferroelectric layer

Under test by GlobalFoundries, February 2018, on 12n technology



The spontaneous polarization of ferroelectrics reduces gate voltage for switching, hence heat dissipation

# Wavelengths

visible light: down to 390 nm

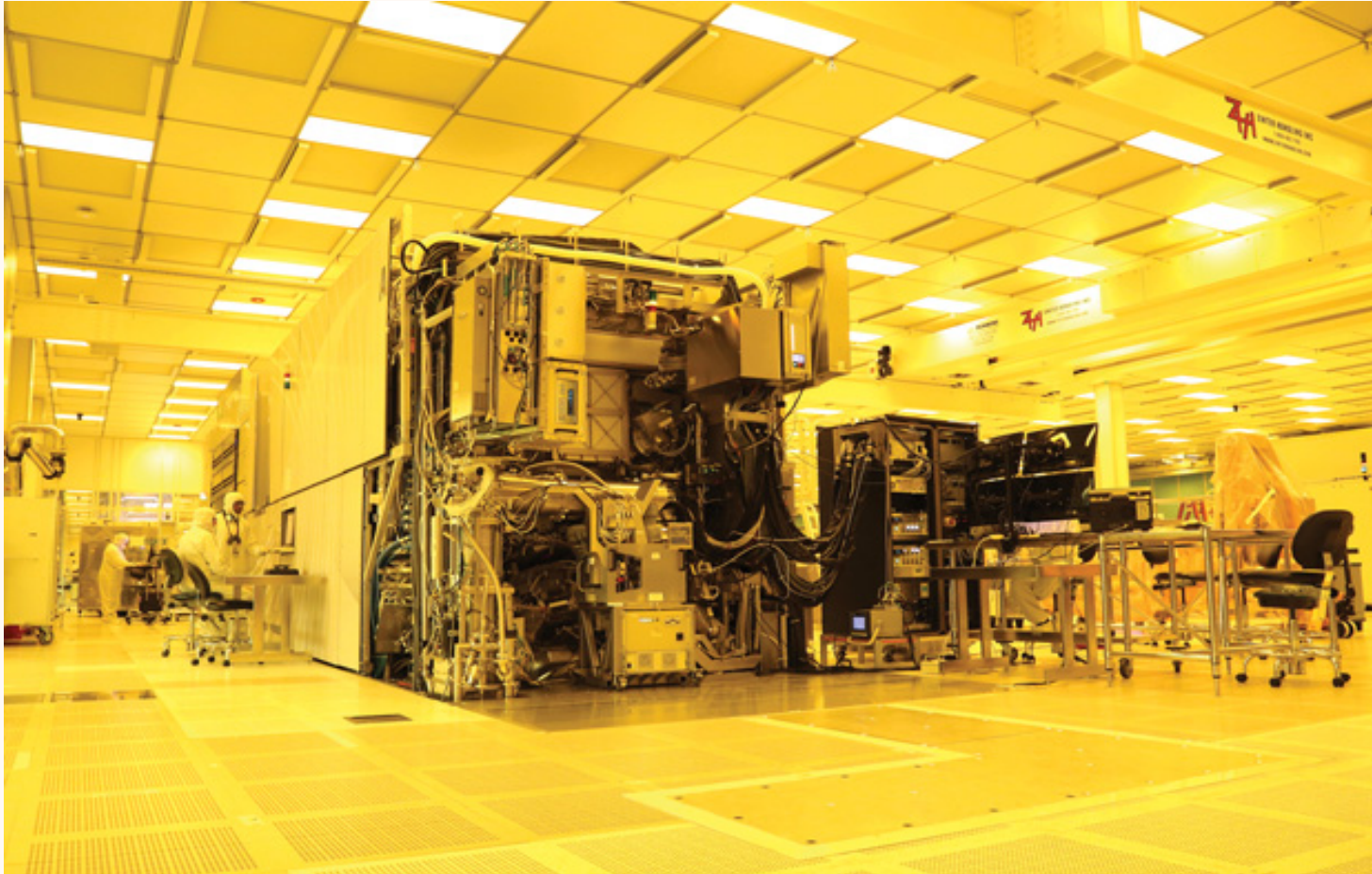
ultraviolet (UV): 380 to 200 nm

extreme ultraviolet (EUV): 200 to 10 nm

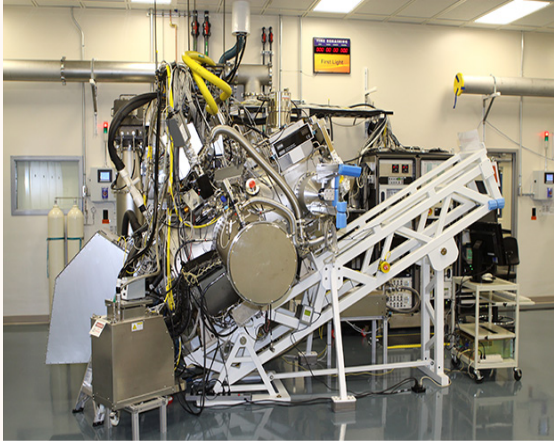
X rays (soft): 10 to 0.1 nm

X rays (hard): below 0.1 nm

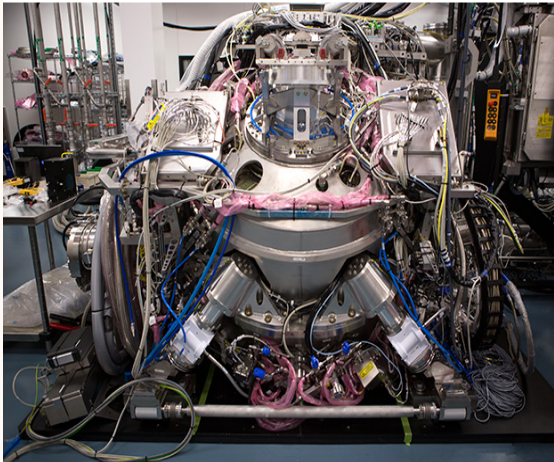




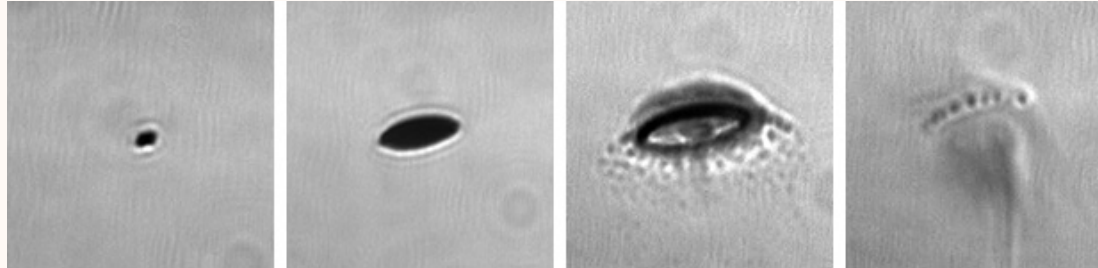
EUV scanner ASML NXE:3300B > 100 M\$ 1.5 MWatt  
SUNY Polytechnic Institute, Albany, NY (2017)



Pulses of laser light are sent into a vessel where they collide with tin droplets

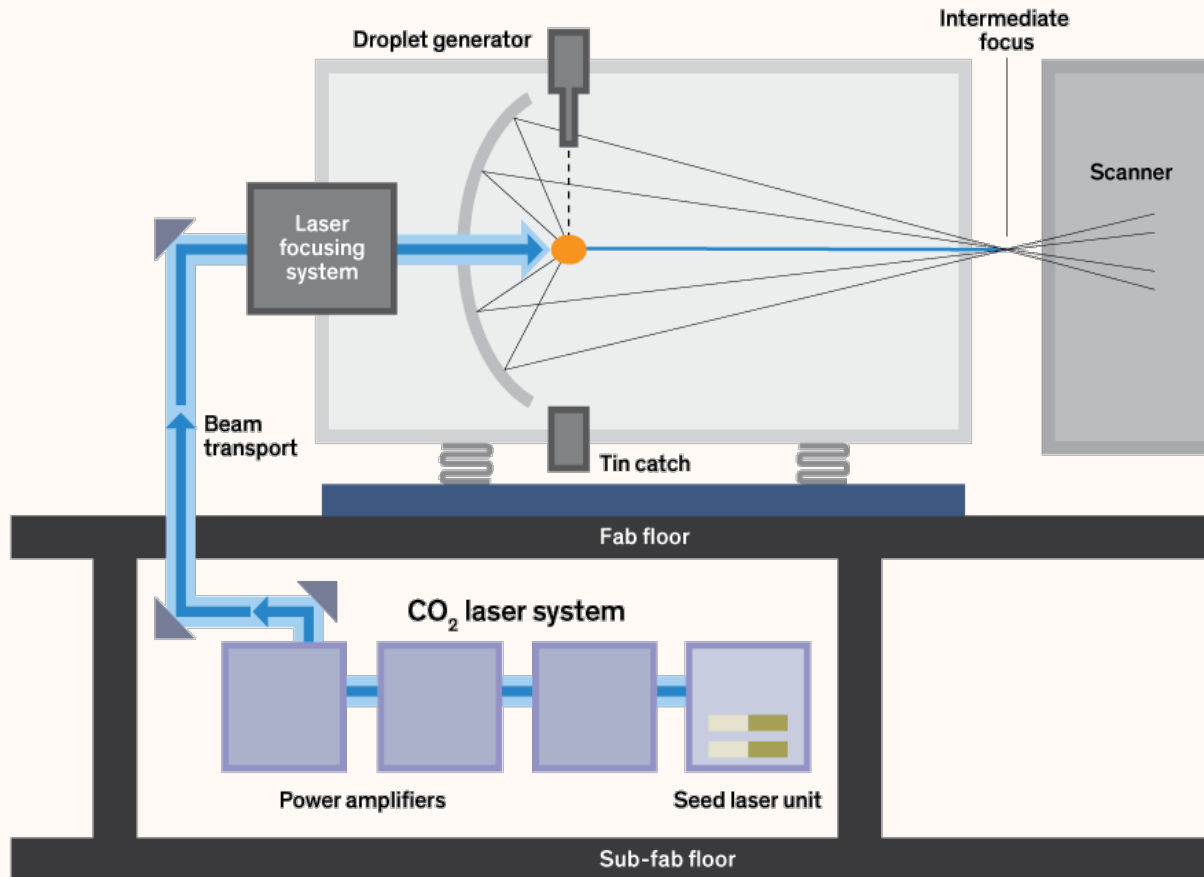


Assembling the scanner



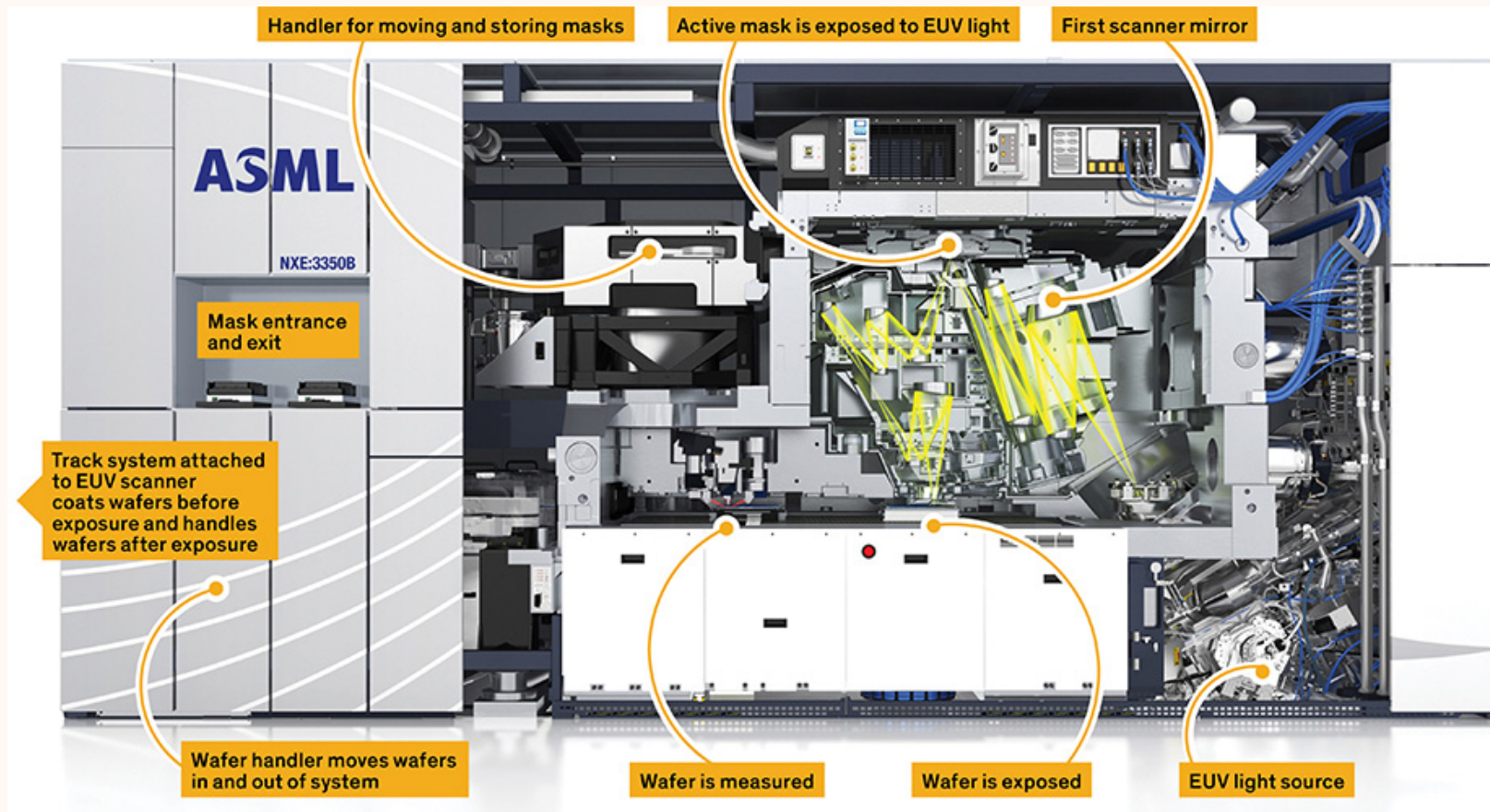
Tin droplets are flattened by one laser pulse  
and then converted to EUV-emitting plasma  
by a second pulse

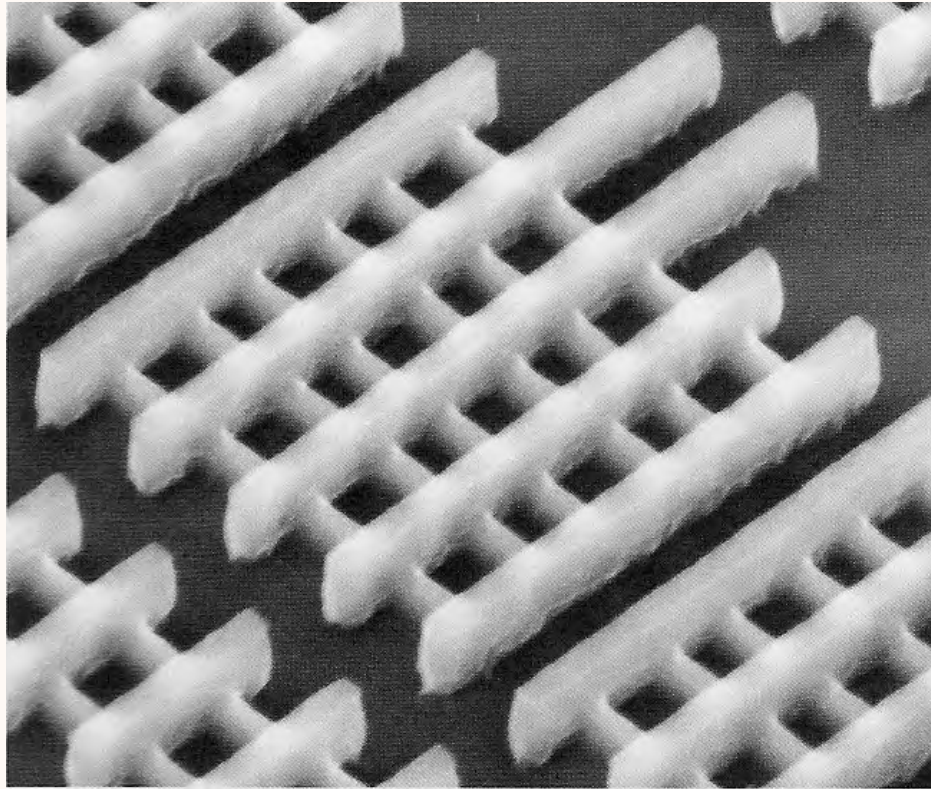
Wavelength 23.5 nm



Generating EUV and focusing through a mirror (Zeiss) made of 40 pairs of alternating silicon and molybdenum layers

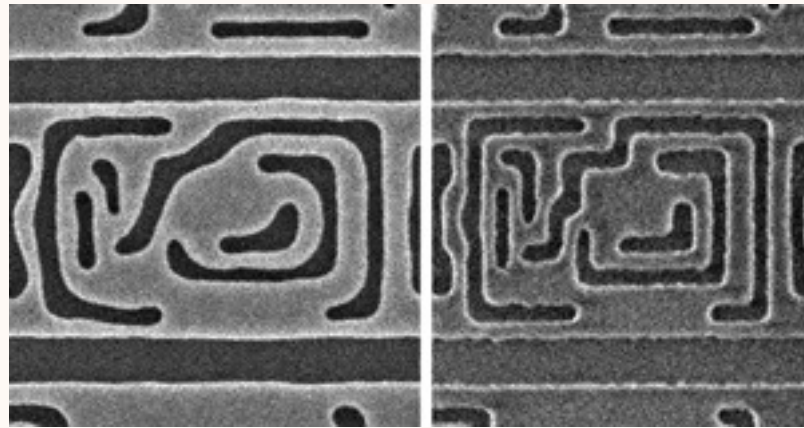






Array of FINFET





light 193 nm

EUV 23.5 nm

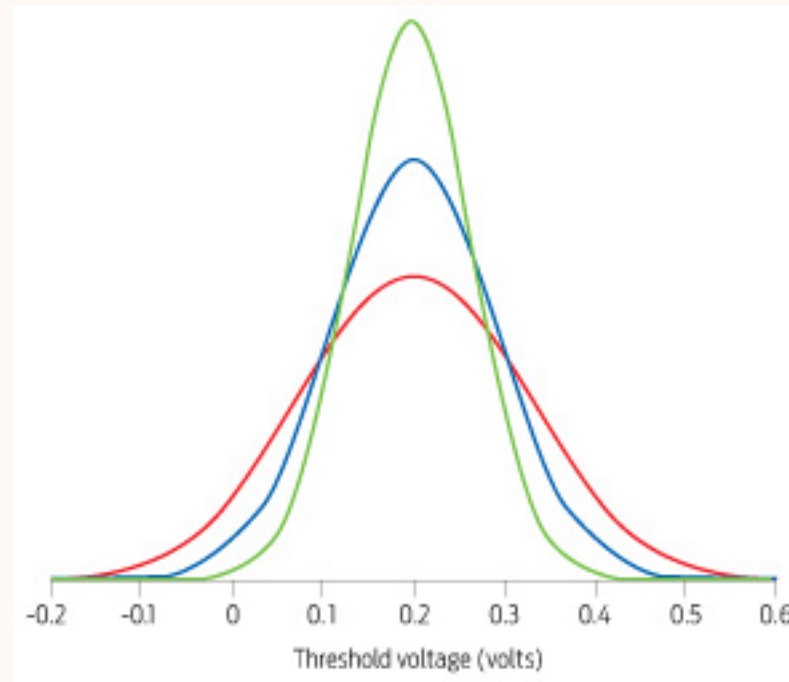
## The effect of impurities

Wafer impurities affect transistor functioning as size gets smaller. Moreover, ion implantation for doping is not too precise when working on an atomic scale.

Recalling that the diameter of a silicon atom is approximately 0.4 nm, the smallest chip details in EUV technology account for a few atoms.

The channel of a FIINFET may contain a few hundred dopant atoms: a difference of few atoms reduces performance .

# Production yield



Threshold voltages to switch transistor green

28nm green 20nm blue 14nm red

As feature sizes get smaller more transistors are unusable

## The problem of connections:

"Wiring is the major bottleneck for semiconductors"

IEEE Int. Electron Devices Meeting

San Francisco, Feb 2018

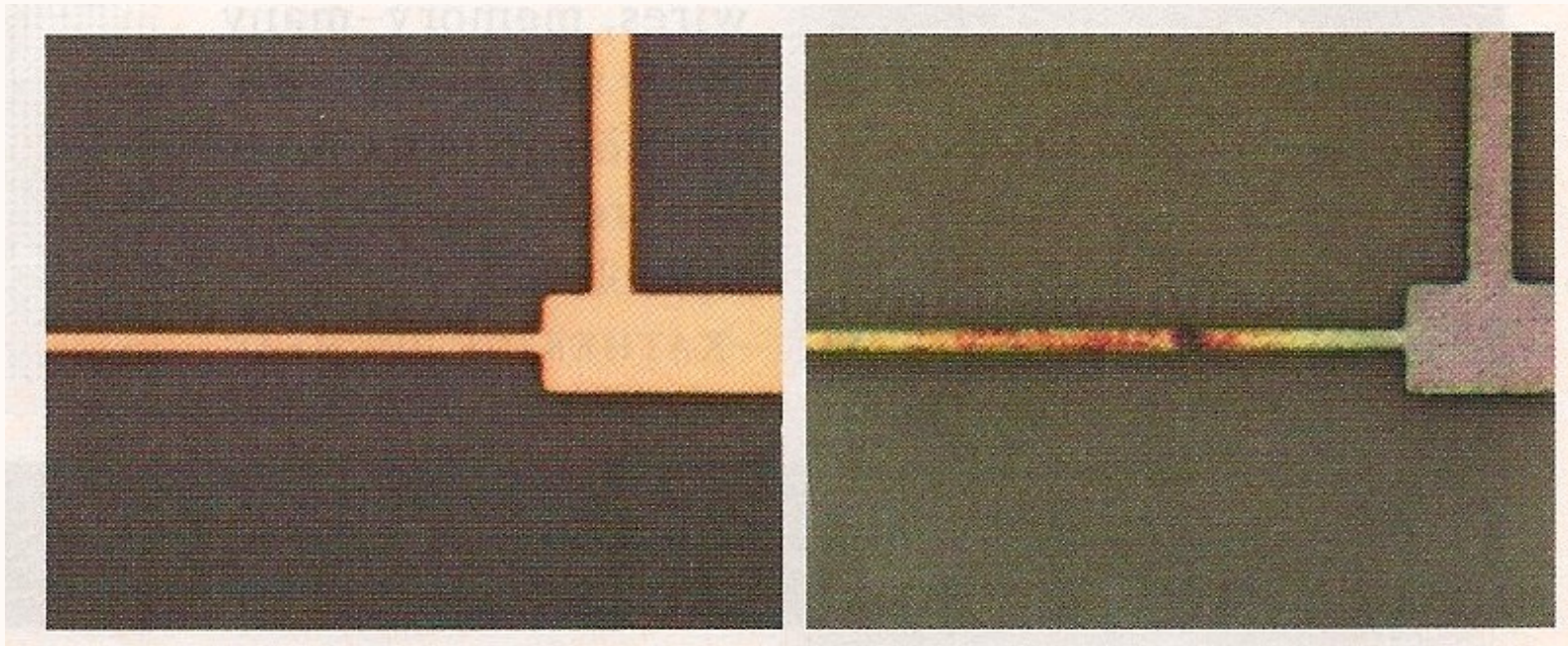
Material used:

from Aluminum (originally) to

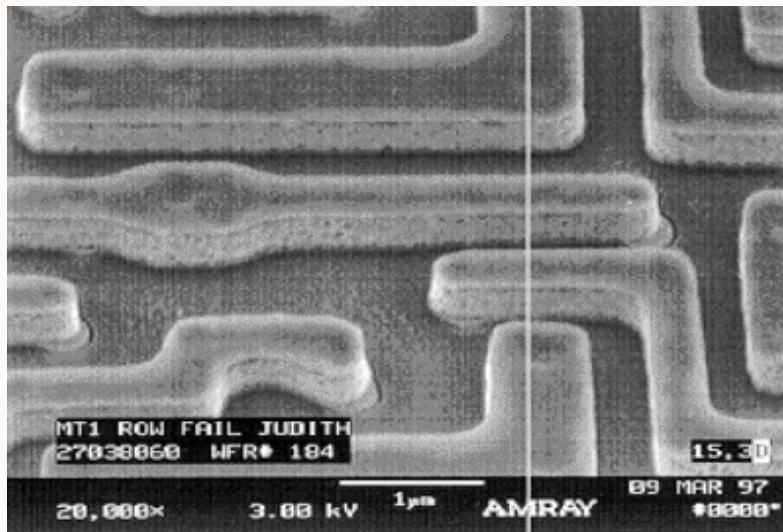
Copper (2000) Tungsten (2005) Cobalt (2015)

Copper has the lowest resistivity but it is prone to **electromigration** (atom dislodge by hitting accelerated electrons) for wires of 10-14 nm

Thin copper interconnection broken by electromigration

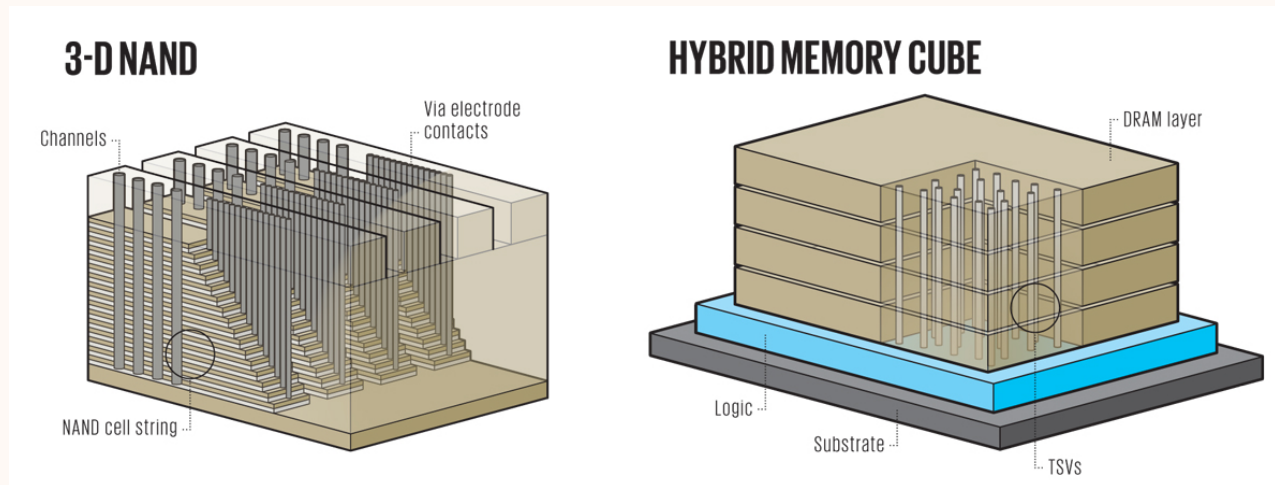


To protect thin copper connections from electromigration, they are lined with a 1-2 nm cobalt or graphene border (2017).





# 3D chips: keeping Moore's law alive



Much shorter connections on the average  
reduce delays

# The new GPS frontier



**SKINNY SIGNALS:** To be accurate, receivers need the signal that takes the shortest path from the satellite [green]. Classic L1 satellite signals overlap with their reflections [blue and purple] to form signal “blobs,” which mask the shortest path. L5 signals don’t overlap with their reflections, so receivers can easily find the signal that arrives first.

