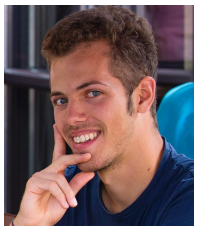
europass Curriculum Vitae

PERSONAL INFORMATION

Federico Mariti



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Date of birth 07/03/1987 | Nationality Italian

EDUCATION AND TRAINING

Sep 06–Jun 13

Bachelor's degree in Computer Science

University of Pisa, Pisa (Italy)

Graduation mark 109/110

Bachelor's Thesis

Run-time support to communication mechanisms for many-core architectures.

Supervisor: prof. Marco Vanneschi.

The work has been carried out at the Department of Computer Science, University of Pisa

Exams with final project

Web Services Laboratory. prof. Tito Flagella

Architectures, protocols and tools for development and implementations of Internet Applications.

Project: web service implementation, with proxy and security mechanisms, for the management of hotel rooms management.

Network Management. prof. Luca Deri

Network management problems, principles and tools that allow the management of complex communication networks. Monitoring needs in heterogeneous networks and available tools.

Project: implementation of a program for performance measurement of network devices with two network interfaces. Usage of PCAP library for the traffic generation.

Operating Systems Laboratory. prof. Susanna Pelagatti

C programming with Unix/POSIX system calls: handling of files and directories, processes, threads, signals, pipes, sockets and various synchronization mechanisms.

Project: implementation of a messaging server.

Introduction to Digital Audio. prof. Francesco Romani

Theoretical and practical foundations of digital audio.

Project: implementation of a Java program for audio signal processing.

Sep 01–Jul 06

High school diploma in Industrial and Technical Institute

Istituto Tecnico Industriale Enrico Fermi, Lucca, Lucca (Italy)

PERSONAL SKILLS

Mother tongue(s) Italian

Other language(s)

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
English	B2	B2	B2	B2	B2

Levels: A1/A2: Basic user - B1/B2: Independent user - C1/C2: Proficient user
Common European Framework of Reference for Languages

Communication skills

Aptitude to communicate in a precise and clear way. This was gained during university studies, developing a passion for the rigor and the formalism. Good relationship and ability to work in a team acquired during the university, confronting with colleagues, and during the apprenticeship period.

Organisational / managerial skills

Excellent ability to plan work independently and design software systems to be accomplished by own account. These capabilities were gained working on apprenticeship and developing exam projects. High ability to deal with new issues through the study of articles, manuals, technical reports, Request For Comments, or other documentations.

Computer skills

Excellent knowledge of programming languages C, C++ and Java. Mastery of Unix and POSIX development environment.

Excellent knowledge of parallel architectures and parallel software development methodologies. Use of FastFlow and OpenMP library.

Good knowledge of architectures, protocols, tools for the development of Web Service. Use of the JEE environment: HTTP, SOAP, WDSL, XML/XSD, Java Servlet, JAXP, JAX-WS, WS-Security, CXF framework.

Thorough knowledge of Internet protocol stack. Use of the PCAP library.

Good knowledge of relational database and SQL language.

Knowledge of cryptographic theoretical foundations and modern security system used in Internet (SSL).

Use of GnuPlot for data presentation. Use of LaTex for drafting documents and reports.

ADDITIONAL INFORMATION

Apprenticeship bachelor degree in Computer Science

Run-time support to communication mechanisms for many-core architectures.

Supervisor: prof. Marco Vanneschi.

The work has been carried out at the Department of Computer Science, University of Pisa.

The advent of multi-/many-core architectures demands efficient run-time supports to sustain parallel applications scalability. In the field of fine grain computations key mechanisms are processes cooperation and processes communication. Peculiar architectural supports such as cache coherence or core interconnection networks can be used to design optimized implementations of such mechanisms. The work has focused on the optimization of processes communication mechanisms in the processor Tilera TilePro64. This processor have an interesting architecture characterised by multiple on-chip core interconnection networks, with mesh topology. Have been realized different versions of communication mechanisms using specific cache coherence techniques and the on-chip interconnection network. The results obtained show that the interconnection network provides better overall performances than the shared memory although with specific caching techniques.

Hobby and Passions

Mountain bike, road bike, photography.

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ANNEXES

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Bachelor of Computer Science

Grades

Exam	Grade	Credit Hrs	Professor
Algebra	28	6	Francesco Paolo Di Stefano
Algorithmic	26	9	Linda Pagli
Databases	26	6	Antonio Albano
Physics	21	6	Alberto Maria Messineo
Programming Fundamentals	28	9	Roberto Barbuti
Introduction to Programming Laboratory	28	6	Andrea Corradini
Data Structures Programming Laboratory	28	3	Francesco Romani
Languages and Methods of Mathematics	28	6	Giovanni Gaiffi
Programming Methodologies	30	6	Marco Bellia
Algorithms for Internet and Web: Critography	30	6	Fabrizio Luccio
Mathematical Analysis	25	8	Mauro Sassetti
Computer Architecture	24	10	Marco Vanneschi
Calculation of Probabilities and Statistics	25	6	Maurizio Pratelli
Numerical Calculation	27	6	Roberto Bevilacqua
Network Management	28	6	Luca Deri
Introduction to Digital Audio	28	3	Francesco Romani
Web Services Laboratory	30L	6	Tito Flagella
System Languages Laboratory	28	3	Vincenzo Gervasi
Concurrent Programming Laboratory	30	6	Susanna Pelagatti
Operational Research	26	6	Giancarlo Bigi
Geographic Information Systems	30L	6	Paolo Mogorovich
Operating Systems	30L	6	Piero Maestrini
Software Engineering	26	6	Carlo Montangero
Network Programming Laboratory	27	6	Vincenzo Gervasi
Logic for the Programming	27	6	Andrea Corradini
Computer Networks	25	6	Antonio Brogi
Apprenticeship	30L	18	Marco Vanneschi
High Performance Computing	30L	9	Marco Vanneschi